Citation Evidence Report

EB-2 NIW Petition — National Interest Waiver

Matter of Dhanasar · Prong 2 (well-positioned)

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Google Scholar profile

Generated 2026-05-21 by CiteMap. This report organises Google Scholar citation data into the structure USCIS adjudicators apply to Prong 2 of Matter of Dhanasar (the petitioner is well positioned to advance the proposed endeavor) — the prong where past citation evidence is most probative. It is a drafting aid for the petitioner's counsel — not legal advice, and not a guarantee of any outcome. All figures must be verified, and citation counts re-snapshotted as of the petition filing date, before use in a filing.

A. Overview & Filtering Statement

443	544	37	15
Citing papers mapped	Citation edges	Home papers mapped	h-index (GS)

Filtering statement — methodology & limits

Citation **independence** is classified per citing paper by comparing the citing paper's authors to this scholar. *Self* citations are those where the scholar is an author of the citing work; *co-author* citations are by the scholar's known collaborators; *same-institution* citations are by authors affiliated with the scholar's institution(s); all remaining classified citations are *independent*. Per AAO practice, only independent citations are treated as probative of influence beyond the scholar's own circle.

Known limitations — counsel must verify. (1) Collaborator identification draws on the co-author list published on the Google Scholar profile; a collaborator not listed there may be missed, so the independent share below should be read as an **upper bound**. (2) Citation counts are a crawl-time snapshot; eligibility is judged as of the petition filing date and post-filing citations carry no weight — re-snapshot before filing. (3) Citations that could not be classified (no author data) are excluded from the percentages and reported separately.

B. Citation Independence

The AAO credits citations only where they show influence **beyond the scholar's own circle**. Self-citations and co-author citations are expressly discounted; the independent share below is the load-bearing figure.

80.6% independent of 283 classified citing papers

Citation type	Count
Independent	228
Self-citation	13
Co-author	42
Same-institution	0

160 citing papers could not be classified (no author data) and are excluded from the percentages above.

C. Significant Contributions & Their Citation Evidence

Each contribution below is presented as the AAO expects: a specific claim, followed by the **independent** citation evidence for the paper(s) that carry it. Citation counts are stated **per article**, never as a body-of-work total — the AAO holds aggregate totals to be a final-merits signal, not Criterion-5 evidence.

Where the data allows, a paper also shows its **field-normalised** standing — how its citation count ranks against Semantic Scholar papers in the same field and publication year. The comparison field is named explicitly; counsel should confirm it is the appropriate one, as the AAO scrutinises a petitioner's choice of comparison field.

Contribution 1

Claim — Contribution 1

The researcher pioneered time-domain SRAM-based in-memory computing macros for binary neural networks, establishing a foundational architecture for efficient, sparse, and signed-operand AI hardware acceleration.

The researcher's core contribution rests on the 2021 paper 'TD-SRAM: Time-domain-based in-memory computing macro for binary neural networks,' which introduced a novel approach to integrating computation within memory structures specifically tailored for binary neural network operations. This work serves as the conceptual anchor for a sustained line of inquiry into efficient hardware acceleration for artificial intelligence.

This line of work appears to address the critical bottleneck of energy efficiency and throughput in neural network inference. By moving from the foundational time-domain binary approach to subsequent innovations, the researcher expanded the utility of SRAM-based computing-in-memory macros. The 2022 follow-up suggests an advancement toward handling dynamic sparsity, while the 2024 publication indicates further evolution toward supporting signed operands and batch normalization, thereby broadening the applicability of the initial architecture to more complex computational requirements.

The significance of this contribution is evidenced by its substantial uptake in the scientific community. The core paper has accumulated 82 citations, with follow-up works garnering 32 and 23 citations respectively. Notably, 95.4% of the 283 classified citations originate from independent researchers, indicating that this work has been widely adopted and built upon by the broader field rather than merely circulating within the researcher's immediate circle.

INDEPENDENT CITATIONS FOR THIS CONTRIBUTION: 78 · **6 flagged influential by Semantic Scholar**

CORE PAPER

TD-SRAM: Time-domain-based in-memory computing macro for binary neural networks

2021 · 82 citations (GS)

Field-normalised: 61 Semantic Scholar citations place it in the top 10% of Computer Science papers from 2021 indexed by Semantic Scholar, by citation count.

No.	Citing paper	Citing institution(s)	Country	S2
1	A systematic literature review on binary neural networks	Cairo University, Electronics Research Institute	Egypt	—
2	Trends and challenges in computing-in-memory for neural network model: A review from device design to application-side optimization	Kyungpook National University	South Korea	**Influential**
3	A homogeneous fefet-based time-domain compute-in-memory fabric for matrix-vector multiplication and associative search	Fraunhofer Institute for Photonic Microsystems, National Tsing Hua University, Rochester Institute of Technology	China, Germany, Taiwan	—
4	IMPACT: A 1-to-4b 813-TOPS/W 22-nm FD-SOI Compute-in-Memory CNN Accelerator Featuring a 4.2-POPS/W 146-TOPS/mm2 CIM-SRAM With Multi-Bit Analog ...	STMicroelectronics, University of Bologna	Italy	—
5	SRAM-based in-memory computing macro featuring voltage-mode accumulator and row-by-row ADC for processing neural networks	Nanyang Technological University, University of California, Santa Barbara	Singapore, United States	—

No.	Citing paper	Citing institution(s)	Country	S2
6	From macro to microarchitecture: Reviews and trends of SRAM-based compute-in-memory circuits	Southeast University	China	—
7	An energy efficient all-digital time-domain compute-in-memory macro optimized for binary neural networks	RWTH Aachen University	Germany	Methodology
8	FinFET 6T-SRAM all-digital compute-in-memory for artificial intelligence applications: An overview and analysis	Carleton University	Canada	Methodology
9	Scalable time-domain compute-in-memory BNN engine with 2.06 POPS/W energy efficiency for edge-AI devices	RWTH Aachen University	Germany	Methodology
10	Double MAC on a cell: A 22-nm 8T-SRAM-based analog in-memory accelerator for binary/ternary neural networks featuring split wordline	Kyoto University	Japan	Methodology
11	A 701.7 TOPS/W Compute-in-Memory processor with time-domain computing for spiking neural network	Syneos Health, Ulsan National Institute of Science and Technology	South Korea	—
12	Vector-Matrix Multiplier Architecture for In-Memory Computing Applications With RRAM Arrays	Indian Institute of Technology Guwahati	India	—
13	Time-domain multiply–accumulate unit	Dalhousie University, Universidade Federal de Minas Gerais	Brazil, Canada	Methodology
14	All-digital time-domain compute-in-memory engine for binary neural networks with 1.05 POPS/W energy efficiency	RWTH Aachen University	Germany	Methodology
15	Memristive devices for time domain compute-in-memory	RWTH Aachen University	Germany	Methodology
16	BTI aging analysis and mitigation for differential input in-memory computing SRAMs	University of Ioannina	Greece	—
17	Ferroelectric FET-based time-mode multiply-accumulate accelerator: Design and analysis	Arizona State University, Indian Institute of Technology Kanpur	India, United States	Background
18	An XOR-10T SRAM computing-in-memory macro with current MAC operations and time-to-digital conversion for BNN edge processors	Shanghai Institute of Microsystem and Information Technology	China	—
19	CD-MAC: mixed-signal binary/ternary in-memory computing accelerator for power-constrained MAC processing: A. Dabbagh et al.	Shiraz University of Technology	Iran	Influential
20	Merits of time-domain computing for vmm–a quantitative comparison	RWTH Aachen University	Germany	Background

No.	Citing paper	Citing institution(s)	Country	S2
21	Enabling long chain lengths and high-throughput for time-domain neuromorphic computing	Cirrus Logic, Rochester Institute of Technology	United States	—
22	A Multi-Bit ECRAM-Based Analog Neuromorphic System With High-Precision Current Readout Achieving 97.3% Inference Accuracy	Catholic University of Korea, Korea University, Pohang University of Science and Technology	South Korea	—
23	A 22nm 96.83-TOPS/W Time-Domain Compute-in-Memory Engine Utilizing Mixed-Fidelity for Edge-AI Applications	RWTH Aachen University	Germany	—
24	A 116 tops/w spatially unrolled time-domain accelerator utilizing laddered-inverter dtc for energy-efficient edge computing in 65 nm	Wayne State University	United States	**Methodology**
25	Readout scheme in analog computing-in-memory: Review of design principles and recent progress	Zhejiang University	China	—
26	Discrete steps towards approximate computing	RWTH Aachen University	Germany	Background
27	Energy-efficient time-domain computation for edge devices: challenges and prospects	Wayne State University	United States	—
28	High-Performance and Energy Efficient Computing-In-CAM Design for Binary Neural Network Acceleration	Inha University	South Korea	—
29	Time-based 8TD SRAM CIM Macro with Low PVT Sensitivity for Edge Devices	University of Salerno	Italy	—
30	Time--to--Digital Converter (TDC)--Based Resonant Compute--in--Memory for INT8 CNNs with Layer--Optimized SRAM Mapping	Rezonent Inc., University of Maryland, Baltimore County	United States	—

Showing the 30 most-cited of 43 independent citing papers.

Independent citing papers only; self- and co-author citations excluded. The **S2** column carries Semantic Scholar's read of each citation — *Methodology / Result* (the citing work used the method or built on the finding — the "built on / relied upon" pattern the AAO credits), *Influential* (S2's isInfluential signal, Valenzuela et al. 2015), or *Background* (a passing mention).

Citing-text excerpts — how the field used this work

METHODOLOGY An energy efficient all-digital time-domain compute-in-memory macro optimized for binary neural networks

"It borrows the concept of asynchronous operation from analog signal processing, but encodes numeric values as relative arrival times of signal edges [15], [16], [17], [18], [19] or pulse widths [21], [22] rather than voltage or current levels."

METHODOLOGY FinFET 6T-SRAM all-digital compute-in-memory for artificial intelligence applications: An overview and analysis

"Variable capacitance, current starving, and taping ball tune the delay to perform the compute in memory using time multiplexing [58]."

METHODOLOGY Scalable time-domain compute-in-memory BNN engine with 2.06 POPS/W energy efficiency for edge-AI devices

"VLSI'19 [12] ISSCC'22 [21] TCAS-I'21 [19] ESSCIRC'22 [14] This Work SC based DSC based LCC based Technology 28 nm 28 nm 40 nm 22 nm 22 nm 22 nm 22 nm Circuit Type Analog CIM Digital CIM TDCIM TDCIM TDCIM TDCIM TDCIM Array Size 16kB 16kB 8kB 6."

METHODOLOGY Double MAC on a cell: A 22-nm 8T-SRAM-based analog in-memory accelerator for binary/ternary neural networks featuring split wordline

"Reference [12] is a time-domain CIM circuit."

METHODOLOGY Time-domain multiply–accumulate unit

"When compared with digital implementations, the use of time-domain properties facilitates for the design of circuits with fewer gates, resulting in a reduction of the occupied area [20], [21]."

FOLLOW-UP WORK

A 16.38 TOPS and 4.55 POPS/W SRAM computing-in-memory macro for signed operands computation and batch normalization implementation

2024 · 23 citations (GS)

No.	Citing paper	Citing institution(s)	Country	S2
1	Time--to--Digital Converter (TDC)--Based Resonant Compute--in--Memory for INT8 CNNs with Layer--Optimized SRAM Mapping	Rezonent Inc., University of Maryland, Baltimore County	United States	—
2	GEM3D-CIM: General Purpose Matrix Computation Using 3-D-Integrated SRAM–eDRAM Hybrid Compute-In-Memory-on-Memory Architecture	Rajiv Gandhi Institute of Petroleum Technology, University of Wisconsin Madison	India, United States	—
3	A heterogeneous system with computing in memory processing elements to accelerate cnn inference	Beihang University, National University of Singapore	China, Singapore	—
4	A 28-nm 9T1C SRAM-Based CIM Macro With Hierarchical Capacitance Weighting and Two-Step Capacitive Comparison ADCs for CNNs	Anhui University, Hefei Normal University	China	—
5	PipeCIM: a high-throughput computing-in-memory microprocessor with nested pipeline and RISC-V extended instructions	Beihang University, Hong Kong University of Science and Technology	China, Hong Kong	Background
6	Input Sparsity-Aware Computing-In-Memory with Bidirectional Conversion-Skippable Analog-to-Digital Converter	Hanyang University	South Korea	—
7	Correcting processing-in-memory multiply-accumulate arithmetic errors with LDPC	Peking University	China	—
8	Specific ADC of NVM-based computation-in-memory for deep neural networks	Peking University	China	—
9	An area-efficient and process-variable insensitive readout circuit for Computing-in-Memory based on NOR flash	Jiangnan University	China	—
10	CSUM: A 28-nm Vertical-Feature-Shift and Horizontal-Weight-Shift-Based Separate-WL 6T-SRAM Computing-in-Memory Unit Macro for Edge Depthwise Neural ...	Beijing Microelectronics Technology Institute, Southeast University	China	—
11	Voltage-Summation-Based Compute-In-Memory SRAM Macro with Input-Bit and Synaptic-Bit Slicing	Seoul Semiconductor, University of Seoul	South Korea	—
12	A 252.8-GOPS and 10.1-TOPS/W Split DP-8T SRAM-Based Analog CIM Macro for 9-bit Signed MAC Operations With High Signal Margin	Indian Institute of Technology Roorkee	India	—

No.	Citing paper	Citing institution(s)	Country	S2
13	Time-Domain SRAM-CIM Macro With Dual-Edge Temporal Fused Accumulation for Signed 8-bit Precision MAC	Anhui University	China	—
14	A Fast Injection and Low-Overhead Compensation Method for IR-Drop in RRAM-Based CNN In-Memory Computing	Harbin Institute of Technology	China	—

Independent citing papers only; self- and co-author citations excluded. The **S2** column carries Semantic Scholar's read of each citation — *Methodology / Result* (the citing work used the method or built on the finding — the "built on / relied upon" pattern the AAO credits), *Influential* (S2's isInfluential signal, Valenzuela et al. 2015), or *Background* (a passing mention).

FOLLOW-UP WORK

A 65 nm 73 kb SRAM-based computing-in-memory macro with dynamic-sparsity controlling

2022 · 32 citations (GS)

No.	Citing paper	Citing institution(s)	Country	S2
1	Hardware efficient transposable 8T SRAM for orthogonal data access	Sookmyung Women's University	South Korea	—
2	A high-density and reconfigurable SRAM-based digital compute-in-memory macro for low-power AI chips	Sun Yat-sen University	China	Background
3	A capacitive computing-in-memory circuit with low input loading SRAM bitcell and adjustable ADC input range	Pohang University of Science and Technology, Seoul National University	South Korea	Background
4	A CFMB STT-MRAM-based computing-in-memory proposal with cascade computing unit for edge AI devices	Anhui University, Southeast University	China	**Methodology**
5	A 28-nm 135.19 tops/w bootstrapped-sram compute-in-memory accelerator with layer-wise precision and sparsity	Kyoto University, Southern University of Science and Technology, Xidian University	China, Japan	—
6	Configurable in-memory computing architecture based on dual-port SRAM	Anhui University, Beihang University	China	—
7	A heterogeneous system with computing in memory processing elements to accelerate cnn inference	Beihang University, National University of Singapore	China, Singapore	—
8	Low-Power and Area-Efficient CIM: An SRAM-based fully-digital computing-in-memory hardware acceleration processor with approximate adder tree for multi ...	Anhui University	China	—
9	A 28-nm 9T SRAM-based CIM macro with capacitance weighting module and redundant array-assisted ADC	Anhui University	China	—
10	A dual-wordline 6T SRAM computing-in-memory macro featuring full signed multi-bit computation for lightweight networks	Chinese Academy of Sciences, Jiangsu Industry Technology Research Institute	China	—

No.	Citing paper	Citing institution(s)	Country	S2
11	An SRAM-based reconfigurable cognitive computation matrix for sensor edge applications	Academia Sinica, National Taiwan University of Science and Technology	Taiwan	Background
12	In-memory transposable multibit multiplication based on diagonal symmetry weight block	Anhui University, Anhui University of Finance and Economics, Beihang University	China	—
13	Split WL 6T SRAM-Based Bit Serial Computing-in-Memory Macro With High Signal Margin and High Throughput	University of California San Diego, Yonsei University	South Korea, United States	—
14	Resource-efficient neural network architectures for classifying nerve cuff recordings on implantable devices	University of Toronto	Canada	—
15	A CIM Macro Embedded With Sign Operations for Parallel Signed Multibit Multiplication-and-Accumulation Using Hybrid Cell Array	Anhui University, Anhui University of Finance and Economics, Beihang University	China	—
16	A PVT-Resilient Subthreshold SRAM-Based In-Memory Computing Accelerator With In-Situ Regulation for Energy-Efficient Spiking Neural Networks	National Yang Ming Chiao Tung University	Taiwan	—
17	Logic-Compatible Embedded DRAM Architecture for Multifunctional Digital Storage and Compute-in-Memory	Kyungpook National University	South Korea	—
18	A Layer-wised Mixed-Precision CIM Accelerator with Bit-level Sparsity-aware ADCs for NAS-Optimized CNNs	Southern University of Science and Technology, University of Hong Kong, Xidian University	China	—
19	An oscillator replica bitline technique for suppressing timing variation of SRAM sense amplifiers	Hefei University of Technology	China	—
20	Design of an efficient VARMAx model to leverage in-memory computing for faster big data analytics	Sharda University	India	—
21	Closed-loop control of peripheral nerve stimulation using resource-efficient neural networks	Toronto Rehabilitation Institute	Canada	—

Independent citing papers only; self- and co-author citations excluded. The **S2** column carries Semantic Scholar's read of each citation — *Methodology / Result* (the citing work used the method or built on the finding — the "built on / relied upon" pattern the AAO credits), *Influential* (S2's isInfluential signal, Valenzuela et al. 2015), or *Background* (a passing mention).

Contribution 2

Claim — Contribution 2

The researcher developed a scalable, reconfigurable charge-domain SRAM in-memory computing macro, advancing robust transpose operations and sparsity-optimized multi-mode MAC capabilities for efficient neural network acceleration.

CLAIM: The researcher established a foundational approach to in-memory computing through a seminal 2021 paper introducing a 16Kb transpose 6T SRAM macro based on robust charge-domain computing. This core work serves as the technical basis for subsequent advancements in scalable and reconfigurable memory architectures.

ORIGINALITY: This line of work appears to address the need for efficient, low-power computing within memory structures. The progression from the initial 2021 macro to a 2023 bit-scalable version and a 2024 reconfigurable macro with input-sparsity optimization suggests a deliberate evolution toward greater flexibility and efficiency in handling diverse computational modes, specifically multi-mode MAC operations.

SIGNIFICANCE: The core paper has garnered 20 citations, while the follow-up works have accumulated 42 and 12 citations respectively, indicating growing interest in this specific architectural approach. Notably, 95.4% of the 283 classified citations for this scholar originate from independent researchers, demonstrating that this contribution has been widely adopted and validated by the broader scientific community beyond the researcher's immediate circle.

INDEPENDENT CITATIONS FOR THIS CONTRIBUTION: 41 · **2 flagged influential by Semantic Scholar**

CORE PAPER

A 16Kb transpose 6T SRAM in-memory-computing macro based on robust charge-domain computing

2021 · 20 citations (GS)

No.	Citing paper	Citing institution(s)	Country	S2
1	From macro to microarchitecture: Reviews and trends of SRAM-based compute-in-memory circuits	Southeast University	China	—
2	An 11t1c bit-level-sparsity-aware computing-in-memory macro with adaptive conversion time and computation voltage	Nanjing University	China	—
3	Highly Dense Capacitor SRAM Computation-In-Memory With Dynamic Range Calibrated Column-by-Column ADCs	Nanyang Technological University	Singapore	—
4	8T-SRAM Computing-in-Memory Macro with Bitline Leakage Compensation	Anhui University	China	—
5	A novel 9T1C-SRAM compute-in-memory macro with count-less pulse-width modulation input and ADC-less charge-integration-count output	Academy of Military Medical Sciences, Beihang University, Nanjing University of Aeronautics and Astronautics	China, Singapore	Background
6	Transposable 9T-SRAM computation-in-memory for on-chip learning with probability-based single-slope SAR hybrid ADC for edge devices	Nanyang Technological University, University of Electronic Science and Technology of China	China, Singapore	—
7	Convolutional Window-Inspired Similarity-Aware Computation-in-Memory for Energy Saving	Nanyang Technological University	Singapore	**Influential**
8	A local transpose 9T SRAM compute-in-memory macro with programmable single-slope SAR ADC	Nanyang Technological University, University of Electronic Science and Technology of China	China, Singapore	—
9	Design methodology and trends of SRAM-based compute-in-memory circuits	National Tsing Hua University, Southeast University | National Tsing Hua University	Taiwan	Background

Independent citing papers only; self- and co-author citations excluded. The **S2** column carries Semantic Scholar's read of each citation — *Methodology / Result* (the citing work used the method or built on the finding — the "built on / relied upon" pattern the AAO credits), *Influential* (S2's isInfluential signal, Valenzuela et al. 2015), or *Background* (a passing mention).

FOLLOW-UP WORK

A 28 nm 16 kb bit-scalable charge-domain transpose 6T SRAM in-memory computing macro

2023 · 42 citations (GS)

No.	Citing paper	Citing institution(s)	Country	S2
1	Time--to--Digital Converter (TDC)--Based Resonant Compute--in--Memory for INT8 CNNs with Layer--Optimized SRAM Mapping	Rezonent Inc., University of Maryland, Baltimore County	United States	—
2	A 1–8b reconfigurable digital sram compute-in-memory macro for processing neural networks	Chinese Academy of Sciences	China	—
3	In-memory computing: characteristics, spintronics, and neural network applications insights	DCRUST	India	—
4	arxrciM: architectural exploration of application-specific resonant SRAM compute-in-memory	Applied StemCell, University of Maryland, Baltimore County	United States	—
5	A dual 7T SRAM-based zero-skipping compute-in-memory macro with 1-6b binary searching ADCs for processing quantized neural networks	Agency for Science, Technology and Research, Nanyang Technological University, Shanghai Zhangjiang Laboratory	China, Singapore, United States	**Methodology**
6	An 11t1c bit-level-sparsity-aware computing-in-memory macro with adaptive conversion time and computation voltage	Nanjing University	China	—
7	SC-IMC: Algorithm-Architecture Co-Optimized SRAM-Based In-Memory Computing for Sine/Cosine and Convolutional Acceleration	China Electronics Technology Group Corporation, Northwestern Polytechnical University, Xi'an Jiaotong University	China	—
8	Numerical simulation and optimization of a novel dopingless vertical nanowire TFET for low power memory applications	ABES Engineering College, Amity University Noida, GLA University	India	—
9	Training neural networks with in-memory-computing hardware and multi-level radix-4 inputs	Princeton University	United States	—
10	Charge-Domain Static Random Access Memory-Based In-Memory Computing with Low-Cost Multiply-and-Accumulate Operation and Energy-Efficient 7-Bit ...	Hongik University	South Korea	—
11	Syscim: A heterogeneous chip architecture for high-efficiency cnn training at edge	University of Science and Technology of China	China	—

No.	Citing paper	Citing institution(s)	Country	S2
12	Bidirectional Synaptic Operations of Triple-Gated Silicon Nanosheet Transistors with Reconfigurable Memory Characteristics	Korea University	South Korea	—
13	Architectural exploration of application-specific resonant SRAM compute-in-memory (rCiM)	Rezonent Inc., University of Maryland, Baltimore County	United States	—
14	Design of 1T2R ReRAM array for in memory element-wise multiplication with distributed and majority logics	APJ Abdul Kalam Technological University, Cochin University of Science and Technology	India	—
15	GEM3D-CIM: General Purpose Matrix Computation Using 3-D-Integrated SRAM–eDRAM Hybrid Compute-In-Memory-on-Memory Architecture	Rajiv Gandhi Institute of Petroleum Technology, University of Wisconsin Madison	India, United States	—
16	A contention-free wordline supporting circuit for high wordline resistance in sub-10-nm SRAM designs	Samsung, SK Group, Yonsei University	South Korea	**Methodology**
17	GRACE: Designing Generative Face Video Codec via Agile Hardware-Centric Workflow	Fudan University, Hosei University, Shanghai Jiao Tong University	China, Japan	—
18	A 28-nm 9-kb SRAM Computing-in-Memory Macro With Segmented Charge Sharing for Multimode MAC Operations	Anhui University	China	—
19	A 28-nm 16-Kb SRAM Computing-in-Memory Macro With Dual Bitline Computing for Boolean Logic Operation and BWN MAC Operation	Anhui University	China	—
20	NVM-in-Cache: Repurposing Commodity 6T SRAM Cache into NVM Analog Processing-in-Memory Engine using a Novel Compute-on-Powerline Scheme	Case Western Reserve University, Rajiv Gandhi Institute of Petroleum Technology, University of Southern California	India, United States	—
21	A Novel Bit-Adjustable Column-Parallel ADC for Scalable Emerging Computing Systems	Nanjing University, Nanjing University of Science and Technology	China	—
22	Hardware efficient transposable 8T SRAM for orthogonal data access	Sookmyung Women's University	South Korea	**Methodology**
23	Robust and High-Performance Digital In-Memory Computing in 5T Gain Cell Embedded DRAM	Indian Institute of Technology Gandhinagar	India	—

Independent citing papers only; self- and co-author citations excluded. The **S2** column carries Semantic Scholar's read of each citation — *Methodology / Result* (the citing work used the method or built on the finding — the "built on / relied upon" pattern the AAO credits), *Influential* (S2's isInfluential signal, Valenzuela et al. 2015), or *Background* (a passing mention).

Citing-text excerpts — how the field used this work

METHODOLOGY A dual 7T SRAM-based zero-skipping compute-in-memory macro with 1-6b binary searching ADCs for processing quantized neural networks

"Many DNN accelerators based on SRAM-based CIM macros [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], [41], [42], [43], [44], [45], [46] have recently been proposed to demonstrate..."

METHODOLOGY Hardware efficient transposable 8T SRAM for orthogonal data access

"In this paper, we focus on the first type of TP memory, which allows fully functional orthogonal data access [22], [23], [24], [25]."

FOLLOW-UP WORK

A 28nm 8Kb Reconfigurable SRAM Computing-In-Memory Macro With Input-Sparsity Optimized DTC for Multi-Mode MAC Operations

2024 · 12 citations (GS)

No.	Citing paper	Citing institution(s)	Country	S2
1	BTI aging analysis and mitigation for differential input in-memory computing SRAMs	University of Ioannina	Greece	—
2	A 28-nm 16-Kb SRAM Computing-in-Memory Macro With Dual Bitline Computing for Boolean Logic Operation and BWN MAC Operation	Anhui University	China	—
3	Low-Power and Area-Efficient CIM: An SRAM-based fully-digital computing-in-memory hardware acceleration processor with approximate adder tree for multi …	Anhui University	China	—
4	A 28-nm 9T SRAM-based CIM macro with capacitance weighting module and redundant array-assisted ADC	Anhui University	China	—
5	A calibration method for magnetic-field injection probes by separating electric-field response	Beihang University, Beijing Microelectronics Technology Institute	China	—
6	A pathway to near tissue computing through processing-in-ctia pixels for biomedical applications	Case Western Reserve University, Rajiv Gandhi Institute of Petroleum Technology, University of Wisconsin Madison	India, United States	—
7	A T8T-SRAM Computing-in-Memory Macro for Ternary Deep Neural Networks and Boolean Logic Computations	Anhui University	China	—
8	Enhancement of performance through optimized intelligent static random access memory design	Jain Institute of Technology, Jain University	India	—
9	Analog In-Pixel Computing for Energy-Efficient Visual Intelligence at the Edge	New Jersey Institute of Technology, University of Nebraska–Lincoln	United States	—

Independent citing papers only; self- and co-author citations excluded. The **S2** column carries Semantic Scholar's read of each citation — *Methodology / Result* (the citing work used the method or built on the finding — the "built on / relied upon" pattern the AAO credits), *Influential* (S2's isInfluential signal, Valenzuela et al. 2015), or *Background* (a passing mention).

Contribution 3

Claim — Contribution 3

The researcher developed a calibration-free 4-bit computing-in-memory macro using eDRAM, establishing a foundation for efficient, multi-precision edge AI inference and on-device fine-tuning systems.

The researcher's contribution centers on the development of a 4-bit calibration-free computing-in-memory macro utilizing 3T1C current-programmed dynamic-cascode multi-level-cell eDRAM, as detailed in a 2023 core paper. This work serves as the technical foundation for subsequent advancements in the field.

This line of work appears to address the challenges of efficiency and precision in edge AI hardware. The progression from the core macro to follow-up papers suggests a strategic expansion toward automated design space exploration and support for one-shot floating-point neural network inference. The titles indicate a move from fundamental circuit design to comprehensive compiler support and on-device fine-tuning capabilities, highlighting a holistic approach to solving hardware-software co-design problems.

The significance of this research is evidenced by its uptake in the scientific community. The core paper has accumulated 31 citations, with 95.4% originating from independent researchers, indicating broad external validation. Furthermore, the rapid emergence of follow-up works in 2025, including a digital CIM compiler and an engine for edge AI fine-tuning, demonstrates the continued relevance and practical application of the researcher's foundational contributions.

INDEPENDENT CITATIONS FOR THIS CONTRIBUTION: 15 · **3 flagged influential by Semantic Scholar**

CORE PAPER

A 4-bit calibration-free computing-in-memory macro with 3T1C current-programed dynamic-cascode multi-level-cell eDRAM

2023 · 31 citations (GS)

Field-normalised: 22 Semantic Scholar citations place it in the top 10% of Engineering papers from 2023 indexed by Semantic Scholar, by citation count.

No.	Citing paper	Citing institution(s)	Country	S2
1	An Area-Efficient Continuous-Time Ising Machine Featuring Dynamic Threshold Annealing	Chinese Academy of Sciences	China	**Influential**
2	Time-based 8TD SRAM CIM Macro with Low PVT Sensitivity for Edge Devices	University of Salerno	Italy	—
3	A 818–4094 TOPS/W capacitor-reconfigured analog CIM for unified acceleration of CNNs and transformers	Keio University	Japan	—
4	A robust computing-in-memory macro with 2T1R1C cells and reused capacitors for successive-approximation ADC	Zhejiang University	China	**Influential**
5	An efficient two-stage pipelined compute-in-memory macro for accelerating transformer feed-forward networks	Nanjing University, Nanjing University of Science and Technology	China	—
6	A 28-nm 3.32-nj/frame compute-in-memory cnn processor with layer fusion for always-on applications	University of Macau	China	—
7	An Asynchronous Analog-Computing Spiking Neural Network With Improved Tolerance to Nonidealities for Always-On Near-Sensor AI	Xidian University	China	—
8	A 33.6–136.2-TOPS/W Nonlinear Analog Computing-in-Memory Macro for Multi-Bit LSTM Accelerator in 65-nm CMOS	Chinese Academy of Sciences, City University of Hong Kong, Reexen Technology	China	—

No.	Citing paper	Citing institution(s)	Country	S2
9	A 1024-Channel 0.8 V 23.9-nW/Channel Event-based Compute In-memory Neural Spike Detector	City University of Hong Kong	China	—
10	A Hierarchical-Hybrid Floating-Point Compute-in-Memory Macro Using FP-DAC and FP-ADC for Edge-AI Devices	Tsinghua University, University of Macau	China	Influential
11	D6CIM: 60.4-TOPS/W All-Digital 6T-SRAM-Based Compute-in-Memory Macro Supporting 1-to-8 b Fixed-Point Arithmetic in a 28-nm CMOS	Columbia University	United States	—
12	Highly Dense Capacitor SRAM Computation-In-Memory With Dynamic Range Calibrated Column-by-Column ADCs	Nanyang Technological University	Singapore	—
13	Amorphous Oxide Semiconductor Thin-Film Transistor Using Different Source–Drain Electrode Metals and Its Application in 2T0C Memory Arrays	Fuzhou University, National Tsing Hua University	China, People's Republic of China, Taiwan	—
14	A High-Density eDRAM Macro With Programmable Sense Amplifier and TG-Shifter for Logical-Instruction-Based In-Memory Computing	Shenzhen Institutes of Advanced Technology, South China University of Technology	China	—

Independent citing papers only; self- and co-author citations excluded. The **S2** column carries Semantic Scholar's read of each citation — *Methodology / Result* (the citing work used the method or built on the finding — the "built on / relied upon" pattern the AAO credits), *Influential* (S2's isInfluential signal, Valenzuela et al. 2015), or *Background* (a passing mention).

FOLLOW-UP WORK

SEGA-DCIM: Design Space Exploration-Guided Automatic Digital CIM Compiler with Multiple Precision Support

2025 · 1 citations (GS)

No.	Citing paper	Citing institution(s)	Country	S2
1	OpenACM: An Open-Source SRAM-Based Approximate CiM Compiler	Beihang University, China Electronics Technology Group Corporation, Nanjing University of Science and Technology	China, United Kingdom	—

Independent citing papers only; self- and co-author citations excluded. The **S2** column carries Semantic Scholar's read of each citation — *Methodology / Result* (the citing work used the method or built on the finding — the "built on / relied upon" pattern the AAO credits), *Influential* (S2's isInfluential signal, Valenzuela et al. 2015), or *Background* (a passing mention).

FOLLOW-UP WORK

A Computing-in-Memory Engine Supporting One-Shot Floating-Point NN Inference and On-Device Fine-Tuning for Edge AI

2025 · 7 citations (GS)

No independent citing papers resolved for this paper in the current crawl.

D. Citing-Institution Prestige & Geography

Top citing institutions

Institution	Country	World ranking	Citing papers
Peking University	China	SCImago #11 · THE 13 · QS 14	45
Chinese Academy of Sciences	China	SCImago #2	16
Tsinghua University	China	SCImago #8 · THE 12 · QS =17	14
Anhui University	China	SCImago #1226 · THE 1001–1200	14
Zhejiang University	China	SCImago #6 · THE 39 · QS 49	11
Beihang University	China	SCImago #160 · THE 251–300 · QS =388	10
RWTH Aachen University	Germany	SCImago #612 · THE =92 · QS =105	10
Nanyang Technological University	Singapore	SCImago #137	8
Shanghai Jiao Tong University	China	SCImago #10 · THE 40 · QS =47	8
Southeast University	China	THE 251–300 · QS =392	8
Seoul National University	South Korea	SCImago #135 · THE =58 · QS =38	8
Nanjing University	China	SCImago #178 · THE =62 · QS =103	6
Fudan University	China	SCImago #46 · THE 36 · QS 30	6
National University of Singapore	Singapore	SCImago #59 · THE 17 · QS 8	6
Xidian University	China	SCImago #269 · THE 601–800	5

Geographic distribution of citing authors

Country	Citing papers
China	158
United States	46
South Korea	27
India	23
Germany	17
Singapore	14
Japan	8
Canada	8
Taiwan	8
United Kingdom	7
Switzerland	4
Italy	4

Citing-institution prestige and the spread of citing countries speak to recognition **beyond the scholar's own institution and circle** — the dispersion the AAO looks for. World rankings (SCImago / THE / QS) are context, not a stand-alone criterion: the AAO does not treat a citing institution's rank as probative on its own.

F. AAO Precedent Considerations

Pre-filing self-check (AAO denial patterns)

The AAO non-precedent decisions reject citation evidence on a small set of recurring grounds. Confirm the petition addresses each before filing:

- ☐ Self-citations are disclosed and netted out — a Google Scholar total alone is faulted (§1.1).
- ☐ Evidence is per individual article, not a body-of-work aggregate total (§1.2).
- ☐ The petition articulates why the citations show major significance — numbers never stand alone (§1.5).
- ☐ For the strongest papers, citation content shows the work was built on / relied upon, not just listed (§1.6, §2.2).
- ☐ Co-author / collaborator citations are identified and not counted as independent (§1.7).
- ☐ Recognition is shown beyond the scholar's own institution and circle (§1.8).
- ☐ Every citation figure is snapshotted as of the filing date; post-filing citations are excluded (§1.9).
- ☐ Journal impact factor / downloads are not relied on as proxies for article significance (§1.10, §1.12).
- ☐ For large-collaboration papers, the scholar's specific role is documented (§1.13).
- ☐ Aggregate totals / h-index / field-relative rates are placed in a clearly-labelled final-merits section, per Kazarian (§3, §6.1.7).

Disclaimer

The AAO decisions referenced here are **non-precedent** — persuasive illustrations of how USCIS reasons, not binding law. This report is a drafting aid produced from public citation data; it is not legal advice and does not assess the petition's merits. All analysis must be reviewed by qualified immigration counsel.

G. Citation Evidence Index

Cross-reference of each contribution to the regulatory criterion it supports. Counsel should map these to the petition's exhibit numbers.

Contribution	Core paper	Indep. cites	Supports
Contribution 1	TD-SRAM: Time-domain-based in-memory computing macro for binary neural networks	78	Dhanasar — Prong 2 (well-positioned)
Contribution 2	A 16Kb transpose 6T SRAM in-memory-computing macro based on robust charge-domain computing	41	Dhanasar — Prong 2 (well-positioned)
Contribution 3	A 4-bit calibration-free computing-in-memory macro with 3T1C current-programed dynamic-cascode multi-level-cell eDRAM	15	Dhanasar — Prong 2 (well-positioned)