Citation Evidence Report

EB-2 NIW Petition — National Interest Waiver

Matter of Dhanasar · Prong 2 (well-positioned)

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Google Scholar profile

Generated 2026-05-21 by CiteMap. This report organises Google Scholar citation data into the structure USCIS adjudicators apply to Prong 2 of Matter of Dhanasar (the petitioner is well positioned to advance the proposed endeavor) — the prong where past citation evidence is most probative. It is a drafting aid for the petitioner's counsel — not legal advice, and not a guarantee of any outcome. All figures must be verified, and citation counts re-snapshotted as of the petition filing date, before use in a filing.

A. Overview & Filtering Statement

272	395	23	8
Citing papers mapped	Citation edges	Home papers mapped	h-index (GS)

Filtering statement — methodology & limits

Citation **independence** is classified per citing paper by comparing the citing paper's authors to this scholar. *Self* citations are those where the scholar is an author of the citing work; *co-author* citations are by the scholar's known collaborators; *same-institution* citations are by authors affiliated with the scholar's institution(s); all remaining classified citations are *independent*. Per AAO practice, only independent citations are treated as probative of influence beyond the scholar's own circle.

Known limitations — counsel must verify. (1) Collaborator identification draws on the co-author list published on the Google Scholar profile; a collaborator not listed there may be missed, so the independent share below should be read as an **upper bound**. (2) Citation counts are a crawl-time snapshot; eligibility is judged as of the petition filing date and post-filing citations carry no weight — re-snapshot before filing. (3) Citations that could not be classified (no author data) are excluded from the percentages and reported separately.

B. Citation Independence

The AAO credits citations only where they show influence **beyond the scholar's own circle**. Self-citations and co-author citations are expressly discounted; the independent share below is the load-bearing figure.

78.8% independent of 208 classified citing papers

Citation type	Count
Independent	164
Self-citation	11
Co-author	33
Same-institution	0

64 citing papers could not be classified (no author data) and are excluded from the percentages above.

C. Significant Contributions & Their Citation Evidence

Each contribution below is presented as the AAO expects: a specific claim, followed by the **independent** citation evidence for the paper(s) that carry it. Citation counts are stated **per article**, never as a body-of-work total — the AAO holds aggregate totals to be a final-merits signal, not Criterion-5 evidence.

Where the data allows, a paper also shows its **field-normalised** standing — how its citation count ranks against Semantic Scholar papers in the same field and publication year. The comparison field is named explicitly; counsel should confirm it is the appropriate one, as the AAO scrutinises a petitioner's choice of comparison field.

Contribution 1

Claim — Contribution 1

The researcher pioneered graph convolutional networks for automated analog circuit netlist annotation, establishing a foundational framework that subsequent work has extended to hierarchical structures and broader EDA integration.

The researcher established a foundational approach to automated netlist annotation for analog circuits using graph convolutional networks, as demonstrated in the core 2020 paper. This work serves as the primary anchor for a sustained line of inquiry into applying deep learning techniques to electronic design automation tasks.

This line of work appears to address the challenge of structuring complex analog circuit data for machine learning. The progression from the initial 2020 framework to a 2023 paper on hierarchical annotation suggests an evolution toward handling more complex circuit topologies. The 2024 publication further indicates an effort to strengthen the theoretical and practical links between analog design principles and EDA tools.

The significance of this contribution is evidenced by the core paper's 119 citations, indicating strong adoption within the field. Notably, 80.8% of the scholar's total citing papers originate from independent researchers, suggesting that this specific line of work has generated broad interest and utility beyond the researcher's immediate institutional circle.

INDEPENDENT CITATIONS FOR THIS CONTRIBUTION: 96 · **5 flagged influential by Semantic Scholar**

CORE PAPER

GANA: Graph convolutional network based automated netlist annotation for analog circuits

2020 · 2020 Design, Automation & Test in Europe Conference & Exhibition (DATE), 55-60, 2020 · 119 citations (GS)

Field-normalised: 72 Semantic Scholar citations place it in the top 5% of Engineering papers from 2020 indexed by Semantic Scholar, by citation count.

No.	Citing paper	Citing institution(s)	Country	S2
1	Machine learning for electronic design automation: A survey	Chinese University of Hong Kong, Syracuse University, Tsinghua University	China, United States	—
2	Graph neural networks for integrated circuit design, reliability, and security: Survey and tool	Khalifa University, New York University, New York University Abu Dhabi	United Arab Emirates, United Kingdom, United States	—
3	GNN-RE: Graph Neural Networks for Reverse Engineering of Gate-Level Netlists	Khalifa University of Science and Technology, New York University, Texas A&M University, Qualcomm (United States), New York University	United Arab Emirates, United States	—
4	Applications of artificial intelligence on the modeling and optimization for analog and mixed-signal circuits: A review	University of Michigan	United States	Methodology
5	A comprehensive survey on electronic design automation and graph neural networks: Theory and applications	Infineon Technologies AG and Technical University of Munich, Technical University of Munich	Germany	Methodology
6	Hardware trust and assurance through reverse engineering: A tutorial and outlook	University of Florida, Worcester Polytechnic Institute	United States	—

No.	Citing paper	Citing institution(s)	Country	S2
	from image analysis and machine learning perspectives			
7	Ledro: Llm-enhanced design space reduction and optimization for analog circuits	IBM, Massachusetts Institute of Technology	United States	—
8	Schemato–An LLM for netlist-to-schematic conversion	SonyAI, Sony AI, Sony Semiconductor Solutions	Germany, Japan, Switzerland	—
9	Graph neural networks: A powerful and versatile tool for advancing design, reliability, and security of ICs	New York University Abu Dhabi	United Arab Emirates	Background
10	Machine learning in advanced IC design: A methodological survey	Chinese University of Hong Kong, Technical University of Munich	Germany, Hong Kong	Background
11	Recent developments and perspectives on optimization design methods for analog integrated circuits	Xidian University	China	—
12	Deep learning-based image analysis framework for hardware assurance of digital integrated circuits	Nanyang Technological University	Singapore	—
13	Analog layout placement for FinFET technology using reinforcement learning	Memorial University of Newfoundland	Canada	—
14	Dawn: Efficient trojan detection in analog circuits using circuit watermarking and neural twins	—	—	**Methodology**
15	Deep H-GCN: Fast analog IC aging-induced degradation estimation	Chinese University of Hong Kong	Hong Kong	**Methodology**
16	Analog and mixed-signal layout automation using digital place-and-route tools	Nvidia (United States), Stanford University, Stanford University	United States	—
17	Efficient subgraph matching framework for fast subcircuit identification	The Chinese University of Hong Kong, Shenzhen, Zhejiang University	China	—
18	SMART: Graph Learning-Boosted Subcircuit Matching for Large-Scale Analog Circuits	Chinese University of Hong Kong, Chinese University of Hong Kong, Shenzhen, Silicon Technologies (United States)	China, Hong Kong, United States	**Influential**
19	Circuit-gnn: A graph neural network for transistor-level modeling of analog circuit hierarchies	Drexel University	United States	—
20	Hyperef: Spectral hypergraph coarsening by effective-resistance clustering	Stevens Institute of Technology	United States	Background
21	MCE-HGCN: Heterogeneous Graph Convolution Network for Analog IC Matching Constraints Extraction	—	—	—
22	A graph attention network based system for robust analog circuits' structure recognition	—	—	—

No.	Citing paper	Citing institution(s)	Country	S2
	involving a novel data augmentation technique			
23	Transfer of performance models across analog circuit topologies with graph neural networks	Drexel University	United States	**Methodology**
24	Circuit Diagram Retrieval Based on Hierarchical Circuit Graph Representation	Southeast University	China	—
25	Scalable and order invariant analog integrated circuit placement with attention-based graph-to-sequence deep models	—	—	—
26	A survey of analog computing for domain-specific accelerators	—	—	—
27	Asic circuit netlist recognition using graph neural network	Nanyang Technological University	Singapore	—
28	A robust automated analog circuits classification involving a graph neural network and a novel data augmentation strategy	Infineon Technologies (Austria), Norwegian University of Life Sciences, University of Klagenfurt	Austria, Norway	—
29	Abuttable analog cell library and automatic ams layout	Anhui University, BTD Inc, Eastern Institute of Technology	China, New Zealand, United States	—
30	Hybrid utilization of subgraph isomorphism and relational graph convolutional networks for analog functional grouping annotation	Drexel University	United States	**Methodology**

Showing the 30 most-cited of 68 independent citing papers.

Independent citing papers only; self- and co-author citations excluded. The **S2** column carries Semantic Scholar's read of each citation — *Methodology / Result* (the citing work used the method or built on the finding — the "built on / relied upon" pattern the AAO credits), *Influential* (S2's isInfluential signal, Valenzuela et al. 2015), or *Background* (a passing mention).

FOLLOW-UP WORK

GNN-based hierarchical annotation for analog circuits

2023 · IEEE Transactions on Computer-Aided Design of Integrated Circuits and ..., 2023 · 32 citations (GS)

Field-normalised: 26 Semantic Scholar citations place it in the top 10% of Engineering papers from 2023 indexed by Semantic Scholar, by citation count.

No.	Citing paper	Citing institution(s)	Country	S2
1	Graph neural networks for integrated circuit design, reliability, and security: Survey and tool	Khalifa University, New York University, New York University Abu Dhabi	United Arab Emirates, United Kingdom, United States	—
2	Efficient subgraph matching framework for fast subcircuit identification	The Chinese University of Hong Kong, Shenzhen, Zhejiang University	China	**Methodology**
3	SMART: Graph Learning-Boosted Subcircuit Matching for Large-Scale Analog Circuits	Chinese University of Hong Kong, Chinese University of Hong Kong, Shenzhen, Sil-	China, Hong Kong, United States	**Influential**

No.	Citing paper	Citing institution(s)	Country	S2
		icon Technologies (United States)		
4	MCE-HGCN: Heterogeneous Graph Convolution Network for Analog IC Matching Constraints Extraction	—	—	—
5	Ckt2Vec: Efficient Electrical Encoding for Analog Circuit Representations in Vector Space	The Chinese University of Hong Kong	China	—
6	GENIE-ASI: Generative Instruction and Executable Code for Analog Subcircuit Identification	Sony Semiconductor Solutions, Technical University of Munich	Germany, Japan	—
7	H3Match: A Hybrid Heterogeneous Hypergraph Matching Method for Subcircuit Identification	Anhui Polytechnic University, Chinese University of Hong Kong, Shenzhen, Zhejiang University	China	—
8	Subgraph matching-based reference placement for printed circuit board designs: Z. Zhu et al.	Southeast University	China	—
9	MOSTAR: Multi-Stage Hierarchical Bayesian Optimization for Substructure-Aware High-Dimensional Analog Circuit Sizing	Peking University	China	—
10	Analog and Mixed-Signal IC Modeling and Optimization: An Artificial Intelligence Perspective	McMaster University, Memorial University of Newfoundland	Canada	—
11	Graph attention-based symmetry constraint extraction for analog circuits	University of Science and Technology of China	China	**Methodology**
12	Circuit2Graph: Circuits with graph neural networks	Fuzzy Systems Institute, University of Electro-Communications, University of Electro-Communications, Mitsubishi Electric (Japan)	Japan	Background
13	A Multi-Form Optimization Framework for Analog Integrated Circuit Sizing	Leiden University, Leiden University, Xi'an Jiaotong University, Xi'an Jiaotong University	China, Netherlands	—
14	OPT-GCN: A unified and scalable chiplet-based accelerator for high-performance and energy-efficient GCN computation	George Washington University, University of North Carolina at Charlotte	United States	—
15	TROJAN-GUARD: Hardware Trojans Detection Using GNN in RTL Designs	University of Connecticut, University of Minnesota	United States	—
16	Netlistify: Transforming Circuit Schematics into Netlists with Deep Learning	National Yang Ming Chiao Tung University	Taiwan	—
17	Graph Neural Networks Based Analog Circuit Link Prediction	Guangdong Baiyun University, Hangzhou Dianzi University, University of Cambridge	China, United Kingdom	—

No.	Citing paper	Citing institution(s)	Country	S2
18	Denoised Recommendation Model with Collaborative Signal Decoupling	Sichuan University	China	—
19	Trojan Attacks on Graph Convolution Neural Networks for Circuit Analysis	New York University	United Arab Emirates, United States	—
20	GATOR: A Graph Neural Network based Design Anomaly Predictor	Indian Institute of Technology Jodhpur	India	—
21	Equivalent Circuit for Single/Three Phase Magnetic Coupling With Graph Neural Networks	—	—	—
22	Learning from the implicit functional hierarchy in an analog netlist	Technical University of Munich	Germany	**Methodology**
23	Circuit2Graph: Diodes as Asymmetric Directional Nodes	—	—	—
24	A Linear-Regression-Assisted Trimming Scheme for CMOS Voltage Reference	—	—	—
25	Evaluating the Impact of Circuit Representation on LLM-Based Functional Block Recognition in Analogue Circuits	National University of Science and Technology Politehnica Bucharest	Romania	—
26	A hybrid SE-YOLOv5 and GNN-SGCM approach for intelligent table tennis ball positioning and 3D recognition	—	—	—
27	Synthesis of Smart & Intelligent Sensors	Centre National de la Recherche Scientifique, Chimie de la Matière Condensée de Paris, Chimie de la Matière Condensée de Paris, Centre National de la Recherche Scientifique, Commissariat à l'Énergie Atomique et aux Énergies Alternatives, CEA Le Ripault	France, Germany	—

Independent citing papers only; self- and co-author citations excluded. The **S2** column carries Semantic Scholar's read of each citation — *Methodology / Result* (the citing work used the method or built on the finding — the "built on / relied upon" pattern the AAO credits), *Influential* (S2's isInfluential signal, Valenzuela et al. 2015), or *Background* (a passing mention).

Citing-text excerpts — how the field used this work

METHODOLOGY Graph attention-based symmetry constraint extraction for analog circuits

"Besides, integrating GNN with traditional graph-based algorithms achieves the extractions of analog layout constraints at different design levels [25]."

FOLLOW-UP WORK

Reinforcing the Connection between Analog Design and EDA

2024 · 2024 29th Asia and South Pacific Design Automation Conference (ASP-DAC), 665-670, 2024 · 1 citations (GS)

No.	Citing paper	Citing institution(s)	Country	S2
1	A generalized constraint learning and transfer methodology with net-first graph neural network and selective topological search for hierarchical analog/mixed-signal ...	KU Leuven	Belgium	—

Independent citing papers only; self- and co-author citations excluded. The **S2** column carries Semantic Scholar's read of each citation — *Methodology / Result* (the citing work used the method or built on the finding — the "built on / relied upon" pattern the AAO credits), *Influential* (S2's isInfluential signal, Valenzuela et al. 2015), or *Background* (a passing mention).

Contribution 2

Claim — Contribution 2

The researcher developed the ALIGN open-source analog layout generator and advanced the field by integrating machine learning techniques into analog layout automation.

The researcher's contribution centers on the development of the ALIGN open-source analog layout generator, introduced in a 2020 core paper. This work established a foundational tool for the community, which the researcher subsequently expanded upon in 2021 by exploring machine learning techniques within the context of analog layout automation.

This line of work appears to address the challenge of automating complex analog circuit design. By releasing an open-source generator and then investigating machine learning applications, the researcher suggests a progression from providing accessible baseline tools to exploring advanced, data-driven methodologies for improving layout efficiency and quality.

The significance of this contribution is evidenced by its uptake in the broader research community. The core paper has accumulated 12 citations, and notably, 80.8% of the scholar's total citing papers originate from independent researchers. This high degree of citation independence indicates that the ALIGN framework and related methodologies have been adopted and utilized by external groups, validating the work's utility and impact beyond the researcher's immediate circle.

INDEPENDENT CITATIONS FOR THIS CONTRIBUTION: 12

CORE PAPER

The ALIGN open-source analog layout generator: v1. 0 and beyond

2020 · Proceedings of the 39th International Conference on Computer-Aided Design, 1-2, 2020 · 12 citations (GS)

No.	Citing paper	Citing institution(s)	Country	S2
1	Analog integrated circuit routing techniques: An extensive review	Instituto de Telecomunicações	Portugal	—
2	Sageroute: Synergistic analog routing considering geometric and electrical constraints with manual design compatibility	Peking University	China	—
3	Generative ai for analog integrated circuit design: Methodologies and applications	McMaster University	Canada	—
4	Analogxpert: Automating analog topology synthesis by incorporating circuit design expertise into large language models	Microsoft Research Asia, Peking University	China	—
5	Ted: A python-based analog design environment for agile circuit development	Tsinghua University	China	—

No.	Citing paper	Citing institution(s)	Country	S2
6	Sageroute 2.0: Hierarchical analog and mixed signal routing considering versatile routing scenarios	Aquarius (Slovenia), Peking University	China	—
7	MGARoute: Efficient Analog Routing With Multi-Stage Rip-Up and Rerouting Under Geometric and Symmetry Constraints	—	—	—
8	Reinforcement Learning-Driven Net Order Selection for Efficient Analog IC Routing	—	—	—
9	BAG2 assisted hierarchical analog layout synthesis for planar technologies	FH Kärnten, Kwame Nkrumah University of Science and Technology	Austria, Ghana	—
10	BAG2-assisted analog layout synthesis for TSMC 65 nm and GPDK 45 nm	Carinthia University of Applied Sciences, Kwame Nkrumah University of Science and Technology	Austria, Ghana	—
11	AICL Co-Pilot: An Interactive Analog Integrated Circuit Layout Generator	FH Kärnten, Johannes Kepler University of Linz	Austria	—

Independent citing papers only; self- and co-author citations excluded. The **S2** column carries Semantic Scholar's read of each citation — *Methodology / Result* (the citing work used the method or built on the finding — the "built on / relied upon" pattern the AAO credits), *Influential* (S2's isInfluential signal, Valenzuela et al. 2015), or *Background* (a passing mention).

FOLLOW-UP WORK

Machine Learning Techniques in Analog Layout Automation

2021 · Proceedings of the 2021 International Symposium on Physical Design, 71-72, 2021 · 1 citations (GS)

No.	Citing paper	Citing institution(s)	Country	S2
1	Synthesis of Smart & Intelligent Sensors	Centre National de la Recherche Scientifique, Chimie de la Matière Condensée de Paris, Chimie de la Matière Condensée de Paris, Centre National de la Recherche Scientifique, Commissariat à l'Énergie Atomique et aux Énergies Alternatives, CEA Le Ripault	France, Germany	—

Independent citing papers only; self- and co-author citations excluded. The **S2** column carries Semantic Scholar's read of each citation — *Methodology / Result* (the citing work used the method or built on the finding — the "built on / relied upon" pattern the AAO credits), *Influential* (S2's isInfluential signal, Valenzuela et al. 2015), or *Background* (a passing mention).

D. Citing-Institution Prestige & Geography

Top citing institutions

Institution	Country	World ranking	Citing papers
University of Minnesota	United States	SCImago #165 · THE 88 · QS 210	19

Institution	Country	World ranking	Citing papers
Peking University	China	SCImago #11 · THE 13 · QS 14	13
The University of Texas at Austin	United States	THE 50 · QS 68	12
Texas A&M University	United States	THE =151 · QS 144	9
Chinese University of Hong Kong	Hong Kong	—	5
Drexel University	United States	SCImago #1417 · THE 401–500 · QS 711-720	5
The University of Texas at Austin	United States	—	5
National Yang Ming Chiao Tung University	Taiwan	SCImago #976 · THE 401–500 · QS =199	4
Technical University of Munich	Germany	SCImago #187 · THE 27 · QS =22	4
University of Minnesota	United States	—	4
Hong Kong University of Science and Technology	China	SCImago #483 · THE =58 · QS 44	3
Southeast University	China	THE 251–300 · QS =392	3
Instituto de Telecomunicações	Portugal	—	3
Sony Semiconductor Solutions	Japan	—	3
NVIDIA Corporation	United States	—	3

Geographic distribution of citing authors

Country	Citing papers
United States	77
China	49
Germany	15
Taiwan	8
United Kingdom	6
India	6
Austria	6
Japan	5
Canada	5
France	5
Hong Kong	5
United Arab Emirates	5

Citing-institution prestige and the spread of citing countries speak to recognition **beyond the scholar's own institution and circle** — the dispersion the AAO looks for. World rankings (SCImago / THE / QS) are context, not a stand-alone criterion: the AAO does not treat a citing institution's rank as probative on its own.

E. Citation Growth Over Time

Distinct citing papers by publication year. Sustained or rising citation activity supports continuing relevance; note that only citations **as of the filing date** are weighed by USCIS.

F. AAO Precedent Considerations

Pre-filing self-check (AAO denial patterns)

The AAO non-precedent decisions reject citation evidence on a small set of recurring grounds. Confirm the petition addresses each before filing:

- ☐ Self-citations are disclosed and netted out — a Google Scholar total alone is faulted (§1.1).
- ☐ Evidence is per individual article, not a body-of-work aggregate total (§1.2).
- ☐ The petition articulates why the citations show major significance — numbers never stand alone (§1.5).
- ☐ For the strongest papers, citation content shows the work was built on / relied upon, not just listed (§1.6, §2.2).
- ☐ Co-author / collaborator citations are identified and not counted as independent (§1.7).
- ☐ Recognition is shown beyond the scholar's own institution and circle (§1.8).
- ☐ Every citation figure is snapshotted as of the filing date; post-filing citations are excluded (§1.9).
- ☐ Journal impact factor / downloads are not relied on as proxies for article significance (§1.10, §1.12).
- ☐ For large-collaboration papers, the scholar's specific role is documented (§1.13).
- ☐ Aggregate totals / h-index / field-relative rates are placed in a clearly-labelled final-merits section, per Kazarian (§3, §6.1.7).

Disclaimer

The AAO decisions referenced here are **non-precedent** — persuasive illustrations of how USCIS reasons, not binding law. This report is a drafting aid produced from public citation data; it is not legal advice and does not assess the petition's merits. All analysis must be reviewed by qualified immigration counsel.

G. Citation Evidence Index

Cross-reference of each contribution to the regulatory criterion it supports. Counsel should map these to the petition's exhibit numbers.

Contribution	Core paper	Indep. cites	Supports
Contribution 1	GANA: Graph convolutional network based automated netlist annotation for analog circuits	96	Dhanasar — Prong 2 (well-positioned)
Contribution 2	The ALIGN open-source analog layout generator: v1. 0 and beyond	12	Dhanasar — Prong 2 (well-positioned)